REMARKS

Claims 10-15 are pending in the application. By this Preliminary Amendment, claims 1-3, 5 and 7-9 are canceled without prejudice or disclaimer of the subject matter contained therein, and claims 10-15 are added. Favorable reconsideration is respectfully requested in light of the following Remarks.

I. Formal Matters

1. By this Amendment, Page 26 of the specification is amended to indicate that the elements Q36-Q39 are diode-connected transistors, as shown in Figure 9.

In addition, the last paragraph of Page 30 spanning to Page 31 of the specification is also similarly amended to indicate that the elements Q56-Q59 are diode-connected transistors, as shown in Figure 11.

2. The Office action objects to Claims 2, 3, 8 and 9 asserting that these claims are misleading. By this Amendment, Claims 2, 3, 8 and 9 are canceled, thereby rendering the objection moot. Withdrawal of the objection is respectfully requested.

II. The Claims Satisfy the Requirements of 35 USC §112, Second Paragraph

The Office action rejects Claims 1-3, 5 and 7-9 under 35 USC §112, second paragraph asserting that these claims are confusing. By this Amendment, Claim 1-3, 5 and 7-9 are canceled, thereby rendering the rejection moot. Withdrawal of the rejection is respectfully requested.

III. The Claims Define Patentable Subject Matter

The Office Action rejects Claims 1-3, 5 and 7-9 under 35 USC 103(a) over Mihailovits et al. (U.S. Patent No. 5,847,605, hereinafter "Mihailovits") in view of Okanobu (U.S. Patent No. 4,965,528, hereinafter "Okanobu"). The rejection is respectfully traversed.

By this Amendment Claims 1-3, 5 and 7-9 are canceled, thereby rendering the rejection moot. Withdrawal of the rejection is respectfully requested.

Mihailovits appears to disclose a third order filter circuit comprising three stages 260, 270 and 280. The first stage 260 comprises two differential transistor pairs 201, 202 and 203, 204 and a capacitor 240 connected across the output of the first stage. *See Fig. 2; col. 2, lines 30-38.* The second and third stages 270 and 280 have substantially the same layout as the first stage 260. *See col. 2, lines 38-40.* Each stage operates in substantially the same manner with the filter output being taken from the collector of transistors 210 and 211 of the final stage 280. *See col. 2, lines 43-46.*

To control the cutoff frequency electronically, a doublet, tunable low-pass filter circuit is provided comprising two offset differential pairs. The doublet filter circuit comprises a first pair of transistors 501, 502 having different emitter area, but the same emitter area as corresponding transistors 504, 503 in the opposite pair. The ratio of the emitter areas determines the offset voltage. *See Fig. 5; col. 3, lines 15-19; lines 42-55.*

New independent Claim 10, which corresponds to the embodiment of the invention shown in Figure 2, specifies, *inter alia*, a filter circuit including a first circuit connected to a first terminal of a capacitor. The first circuit comprises a first differential circuit connected between a circuit input terminal, a circuit output terminal

and a first terminal of a capacitor. The first differential circuit formed by a first transistor having a base electrode connected to said circuit input terminal and a collector electrode connected to a first power supply, and four diode-connected transistors connected in parallel with each other and each having an emitter electrode connected to an emitter electrode of the first transistor. The first circuit also includes a second differential circuit comprising a second transistor having a base electrode connected to said circuit input terminal and a collector electrode connected to the first power supply, and four diode-connected transistors connected in parallel with each other and each having an emitter electrode connected to an emitter electrode of the second transistor.

The filter circuit further includes a second circuit having an identical configuration as the first circuit including a second circuit output terminal, and a second circuit input terminal, the second circuit, the second circuit connected to a second terminal of the capacitor, wherein the filter circuit serves as a first-order low-pass filter.

New independent Claim 11, which corresponds to the embodiment of the invention shown in Figure 6, specifies, *inter alia*, a filter circuit including a first circuit connected to a first terminal of a capacitor. The first circuit comprises a plurality of fundamental circuits connected in series between a first power supply and a second power supply to form *n* vertical stages, each vertical stage formed by a transistor and four diode-connected transistors connected in parallel with each other, said transistor of said first vertical stage connected in series with said transistors of the 2-*n* vertical stages, said four diode-connected transistors of said first stage connected in series with said

diode-connected transistors of the 2-*n* vertical stages.

The first circuit also includes a second differential circuit comprising a plurality of fundamental circuits connected in series between said first power supply and said second power supply to form *n* vertical stages, each vertical stage formed by a transistor and four diode-connected transistors connected in parallel with each other, said transistor of said first vertical stage connected in series with said transistors of the 2-*n* vertical stages, said four diode-connected transistors of said first stage connected in series with said diode-connected transistors of the 2-*n* vertical stages.

The filter circuit further includes a second circuit having an identical configuration as the first circuit including a second circuit output terminal, and a second circuit input terminal, the second circuit, the second circuit connected to a second terminal of the capacitor, wherein the filter circuit serves as a first-order low-pass filter.

New independent Claim 12, which incorporates the embodiment of the invention shown in Figure 7, specifies, *inter alia*, a filter circuit including a first circuit connected to a first terminal of a capacitor. The first circuit comprises a plurality of fundamental circuits connected in series between a first circuit input terminal and a first circuit output terminal, each fundamental circuit formed by a first transistor and four diode-connected transistors connected in parallel with each other.

The first circuit also includes a second differential circuit a plurality of fundamental circuits connected in parallel with said plurality of fundamental circuits of said first differential circuit and between said first circuit input terminal, said first circuit output terminal, and said

first terminal of said capacitor, each fundamental circuit formed by a second transistor and four diode-connected transistors connected in parallel with each other.

The filter circuit further includes a second circuit having an identical configuration as the first circuit including a second circuit output terminal, and a second circuit input terminal, the second circuit, the second circuit connected to a second terminal of the capacitor, wherein the filter circuit serves as a first-order low-pass filter.

New independent Claim 13, which incorporates the embodiment of the invention shown in Figure 8, specifies, *inter alia*, a filter circuit including a first circuit connected to a first terminal of a capacitor. The first circuit comprises a first differential circuit comprising a plurality of fundamental circuits connected in parallel between a first circuit input terminal and a first circuit output terminal, each fundamental circuit formed by a first transistor and four diode-connected transistors connected in parallel with each other.

The first circuit also includes a second differential circuit comprising a plurality of fundamental circuits connected in parallel with said plurality of fundamental circuits of said first differential circuit and between said first circuit input terminal, said first circuit output terminal, and said first terminal of said capacitor, each fundamental circuit formed by a second transistor and four diode-connected transistors connected in parallel with each other.

The filter circuit further includes a second circuit having an identical configuration as the first circuit including a second circuit output terminal, and a second circuit input terminal, the second circuit, the second circuit

connected to a second terminal of the capacitor, wherein the filter circuit serves as a first-order low-pass filter.

New independent Claim 14, which incorporates the embodiment of the invention shown in Figure 9, specifies, *inter alia*, a filter circuit including a first circuit comprising a first differential circuit formed by a first transistor having a collector electrode connected to a first power supply, and four diode-connected transistors connected in parallel with each other and each having an emitter electrode connected to an emitter electrode of said first transistor.

The first circuit also includes a second differential circuit formed by a second transistor having a collector electrode connected to said first power supply, and four diode-connected transistors connected in parallel with each other and each having an emitter electrode connected to an emitter electrode of said second transistor, an emitter electrode of said second transistor and each of said emitter electrodes of the four diode-connected transistors connected to said second power supply by a second current source. A base electrode of the first transistor in the first differential circuit and base electrodes of the four diode-connected transistors in the second differential circuit connected to a direct-current power supply.

The filter circuit further includes a second circuit having an identical configuration as the first circuit including a second connection node connected to a second circuit output terminal and to a first terminal of a second capacitor, a second terminal of the second capacitor connected to a second circuit input terminal. The second circuit is connected to the direct-current power supply, wherein the filter circuit serves as a first-order high-pass filter.

New independent Claim 15, which incorporates the embodiment of the invention shown in Figure 11, specifies, *inter alia*, a filter circuit including a first circuit comprising a first differential circuit formed by a first transistor having a collector electrode connected to a first power supply, and four diode-connected transistors connected in parallel with each other and each having an emitter electrode connected to an emitter electrode of said first transistor.

A second differential circuit comprises a second transistor having a collector electrode connected to said first power supply, and four diode-connected transistors connected in parallel with each other and each having an emitter electrode connected to an emitter electrode of said second transistor. A base electrode of said first transistor in said first differential circuit and base electrodes of said four diode-connected transistors in said second differential circuit connected to a direct-current power supply. A first connection node is connected to a second circuit output terminal and to a first terminal of a first capacitor, and a second terminal of said first capacitor is connected to a second circuit input terminal.

A second circuit has an identical configuration as the first circuit including a second connection node connected to a first circuit output terminal and to a first terminal of a second capacitor. A second terminal of said second capacitor is connected to a first circuit input terminal, wherein said filter circuit serves as a first-order all-pass filter.

It is respectfully submitted that the features disclosed in Claims 10-15 are not disclosed, taught or suggested in that applied art, taken singly or in combination.

In view of the foregoing, it is respectfully submitted that Claims 10-15 are allowable over the applied art, taken singly or in combination.

V. Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of the application is earnestly solicited.

Should Examiner Englund believe anything further would be desirable in order to place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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